Novel Fabrication Techniques for Infrared Focal Plane Arrays: Growth, Optical Coupling and Read-out Circuit

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Many emerging infrared (IR) sensing applications simultaneously demand a high sensitivity, low noise, large dynamic range, high resolution and high frame rate. Some examples of these applications are day/night persistent surveillance, border patrol and protection, aerial search and rescue, and environmental remote sensing. Hybrid focal plane arrays using a III-V semiconductor sensors matrix and a CMOS read-out circuit have been used successfully in these fields since the 80s due to the high efficiency of quantum wells (QWIPs) and quantum dots photodetectors (QDIPs) and to the reliability of the mature GaAs and Silicon industry. However, an improvement of their operating temperature and sensitivity are required to expand the use of this technology to new applications.

Here, we present the last results from our laboratory in material growth, device processing and read-out circuit development. For the detectors material, the challenge is how to increase the responsivity without increasing the dark current and noise, which are the main drawbacks for the fabrication of a non-cryogenic system. Since QWIPs and QDIPs are now a well-established technology, such improvements are more and more difficult, and therefore we focused on the research of new types of intersubband structures. We developed a new promising photovoltaic structure based on very high-density InAlAs quantum dots, and we started to work on emerging quantum cascade detectors (QCD) and submonolayer quantum-dots infrared photodetectors (SML-QDIPs), using growth optimization and device simulations and testing as a feedback. We already achieved a very low-noise QCD and a SML-QDIP with a very high responsivity (0.5A/W). Since 2D heterostructures like QCDs are insensitive to normal incident radiation, we developed a process to imprint pyramidal corrugations on top of the sensors array to get a high-efficiency optical coupling in a wide range of wavelengths. The process does not use any sub-micron lithography or dry etching, and can be easily reproduced in a laboratory or on a production scale in a very cheap way.

Finally, we designed and tested a digital read-out circuit for low-impedance photodetectors such as our intersubband photodetectors. This small circuit, sizing about 50 um with a 0.18um CMOS technology, overperformed analog circuits like capacitive transimpedance amplifiers (CTIAs) in several aspects: they have a lower noise and a larger dynamic range, do not suffer from saturation problems and don't need a complex and expensive external signal processing. In addition, this circuit can be scaled down using newer CMOS technology, and can thus be employed in high-resolution FPAs.

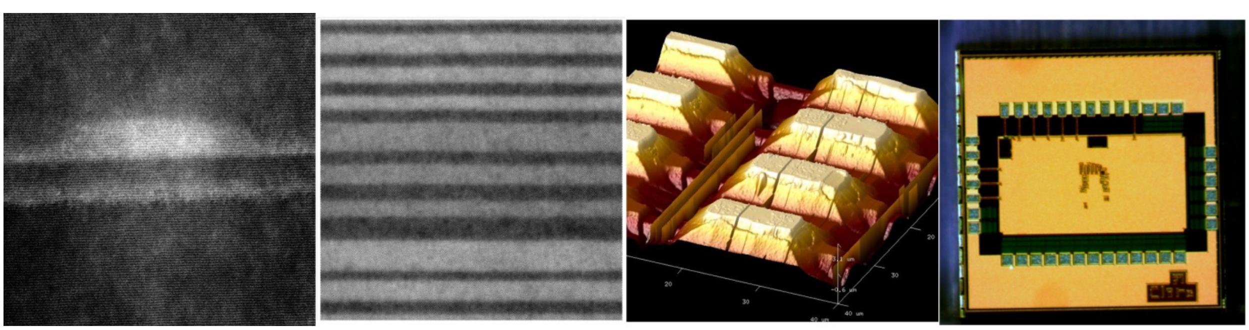

Figure 1: (from left to right) High-resolution transmission electron microscopy image of coupled InAs and InAlAs quantum dots (A, 40 nm x 40 nm) and of a low-noise QCD (B, 50 nm x 50 nm); Atomic –force microscopy image of an array of pyramidally corrugated photodetectors (C, 40 um x 40 um); 1.5 mm x 1.5 mm chip of a digital read-out circuit fabricated by TSMC using 0.18um CMOS technology.